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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/836,480	04/18/2001	Kazutaka Miyano	PNDF-01034	8820
30743	7590	06/10/2005	EXAMINER	
WHITHAM, CURTIS & CHRISTOFFERSON, P.C. 11491 SUNSET HILLS ROAD SUITE 340 RESTON, VA 20190			WANG, TED M	
			ART UNIT	PAPER NUMBER
			2634	

DATE MAILED: 06/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/836,480

Applicant(s)

MIYANO, KAZUTAKA

Examiner

Ted M. Wang

Art Unit

2634

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 January 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 4-6 is/are allowed.
- 6) ☒ Claim(s) 1-3 is/are rejected.
- 7) ☒ Claim(s) 7 and 8 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04 January 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claim 1-3, 7, and 8 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ooishi (US 5,886,946) in view of Yoshimura (US 6,198,322).

- In regard claim 1, Ooishi discloses a PLL circuit comprising:
 - a functional block having a current source (Fig.30 and Fig.43 elements 53 and 54, column 3 line 51 – column 4 line 3, and column 32 lines 45-67); and
 - a bias generation means for generating a constant current source bias signal for controlling the current source of the functional block (Fig.30 and Fig.43 element 52 and column 3 lines 19-61),
 - said bias generation means comprising bias control means which changes the bias signal according to the frequency of the input signal (Fig.30 and Fig.43 element 52 and column 3 lines 19-61, where element 52 is a phase/frequency

comparator generates UP and DOWN control signals to control the current source of the charge pump base on the external clock and internal feedback clock as shown in Fig.30 and Fig.43), and a differential amplifier receiving current from the current source (Fig.30 and Fig.31 element 804, and column 32 line 52 – column 33 line 30).

Ooishi discloses the claimed invention as described as above paragraph except a DLL circuit instead of a PLL circuit. Yoshimura shows that a DLL circuit (Fig.2) has the same function structure as that of a PLL circuit (Fig.1) with substituting the VCO (Fig.1 element 5) to a delay stage (Fig.2 element 4) that is an equivalent structure known in the art. Therefore, because these two (DLL circuit and PLL circuit) were art-recognized equivalents at the time the invention was made, one of ordinary skill in the art would have found it obvious to substitute a delayed stage circuit for VCO.

- In regard claim 2, Ooishi further discloses the limitation that the bias generation means comprises: a first bias generation circuit for generating a primary bias signal corresponding to a predetermined constant current (Fig.30 and Fig.43 elements 51a, 51b, and 53 with UP and /DOWN inputs fixed at a predetermined value); and a second bias generation circuit for generating an internal bias signal based on a bias correction signal output from the bias control means according to the frequency of the primary bias signal and the input signal (Fig.30 and Fig.43 element UP, /DOWN, and 53, and column 3 line 34 – column 4 line 3).

- In regard claim 3, Ooishi further discloses the limitation that the bias control means comprising: measuring means for measuring the frequency of the input signal (Fig.30 and Fig.43 elements 52 with Ext. CLK input and int. CLK); and correction signal generation means for outputting a bias correction signal based on the results of the measurement with the measuring means (Fig.30 and Fig.43 elements 52 output UP and /DOWN).

Allowable Subject Matter

4. Claims 4-6 are allowed.
5. Claims 7 and 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
6. The following is an examiner's statement of reasons for allowance:
 - The examiner's statement of reasons for allowance has been given in the Office action dated 09/29/2004.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

8. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

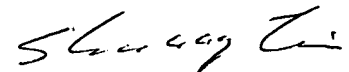
9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted M. Wang whose telephone number is 571-272-3053. The examiner can normally be reached on M-F, 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 571-272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ted M Wang
Examiner
Art Unit 2634

Ted M. Wang



SHUWANG LIU
PRIMARY EXAMINER